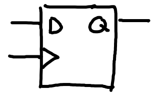
HW 8 Solution

Monday, September 14, 2009
7:00 PM

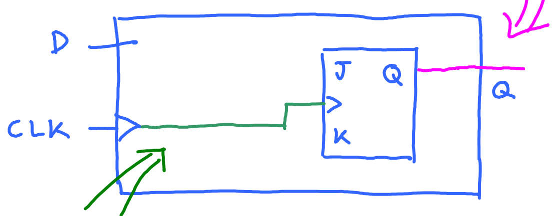
Part A

(1) As a state machine, the D FF has
1 input called D + 1 clock input
1 output called Q



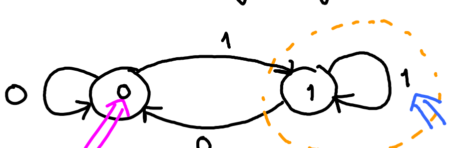
The question specifies that this state machine must be built using J-K FF.

Because the D FF has only two states (which can be considered directly as its output), we will take the output of the J-K FF to be the output of our state machine.



The CLK signal is connected to the clock input of the J-K FF. (This is always the case for synchronous logic design. The clock inputs of all FFs receive the same CLK signal)

We can draw the state diagram from the rule that
"Q will follow D"
on the next rising edge of the clock signal.



The number in here indicate the current state of the J-K FF

The number on the arrow indicate the value of D.

Number 1 on the arrow means D = 1.
Number 1 inside means current Q = 1.
For D FF, we know that the next Q will follow D.
So the next Q = 1. This is

So, the next Q = 1. This is represented by the arrow going back into state value 1.

From the state (transition) diagram, we can read off the values for the next-state table.

We may use the notation Q^* to represent the "next Q".

Input	State	
D	Current Q	Next Q
0	0	0
0	1	0
1	0	1
1	1	1

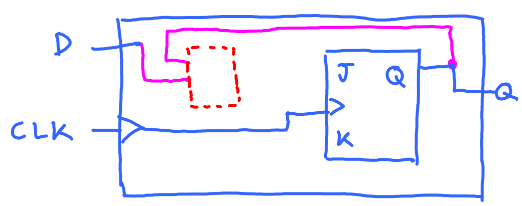
This should read "the next value of Q after the next clock rising edge."

These two columns contain all possible combination of D and "current Q".

(Alternatively, we can copy the value from the D column into the "next Q" column because Q will follow D.)

We use the value of D and the current value of Q to find the next value of Q.

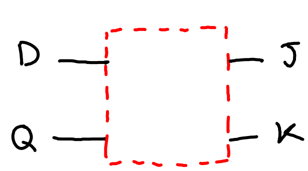
In the circuit below, this is represented by the Q being fed back and the D input being connected into the red box shown in the figure here.



The red box above

1) use the current value of D and Q,
2) calculate what should be the next value of Q according to the next-state table above,
3) control the J, K inputs of the FF so that appropriate next value of Q shows up on the output of the J-K FF.

So, the inputs of the red box are D and Q, the outputs of the red box are J and K.



From the next-state table, we see that

From the next-state table, we see that if $D=0$ and $Q=0$, we want $Q^*=0$. Because Q^* is the output of the JK FF, we need $J=0$ and $K=0$ (hold mode) for the Q^* to stay at the same value as Q. Alternatively, we can make $J=0$ and $K=1$, in which case, Q^* is forced to be 0 because the FF is in RESET mode. In conclusion, if $D=0$ and $Q=0$, we want $J=0$ and $K=X$; that is both $K=0$ and $K=1$ will work. This idea is summarized in the 1st row of the table below

D	Q	Q^*	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

Same reasoning gives the other rows.

This is copied from above

Alternatively, we can use the excitation table for JK FF:

Q	Q^*	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

At this point, we have the following truth table for the red box:

D	Q	J	K
0	0	0	X
0	1	X	1
1	0	1	X
1	1	X	0

K-map for J (rows: D; columns: Q):

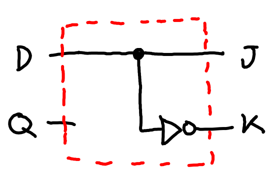
D=0	0	X
D=1	1	X

K-map for K (rows: D; columns: Q):

D=0	X	1
D=1	X	0

K-maps show that $J = D$ and $K = \overline{D}$

Therefore, the red box is simply:



Note the Q (the current state) is not used.

Finally, we put this red box into the circuit that we had drawn before:

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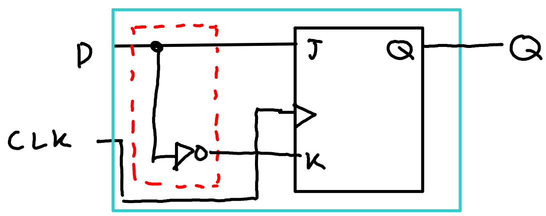


Ans

2) In this problem, there are three states, so two FFs should be enough to represent all three states.

(n FFs can represent 2^n states)

We will take the output of the counter to be the same as the output of the FF. $(Q_1 Q_0)$

Next, we construct the the next-state table from the state transition diagram:

Q_1	Q_0	Q_1^*	Q_0^*
0	0	1	1
0	1	0	0
1	0	X	X
1	1	0	1

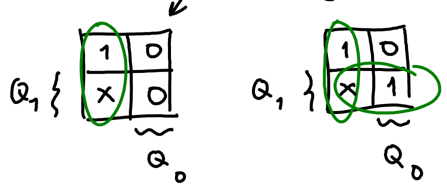
← Again, the * means "next".

The question specifies that we must use D FFs. In general, for D FF, $Q^* = D$. So, from the above table we know that

$$D_1 = Q_1^* \quad \text{and}$$
$$D_0 = Q_0^*.$$

Hence, we have the following truth table for the circuit that compute D_1, D_0 from Q_1, Q_0:

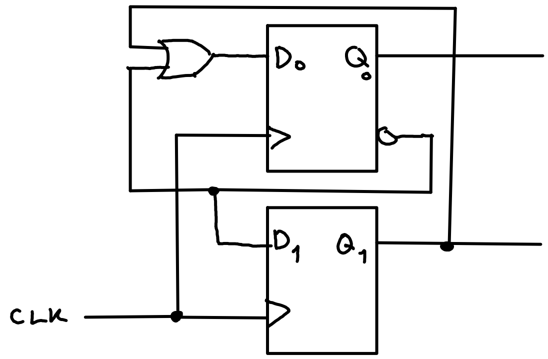
Q_1	Q_0	D_1	D_0
0	0	1	1
0	1	0	0
1	0	x	x
1	1	0	1



K-maps show that $D_1 = \overline{Q_0}$

$$D_0 = \overline{Q_0} + Q_1$$

Hence, our final answer is



Ans

(3) If I solve problem (2) correctly, the only unknown transition now is the transition from state "2" which is left as don't care in the "next-state" table in problem (2).

For state "2", $Q_1 = 1$ and $Q_0 = 0$.

Because $D_1 = \overline{Q_0}$ and $D_0 = \overline{Q_0} + Q_1$, we have

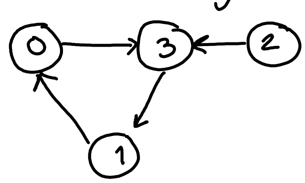
$D_1 = 1$ and $D_0 = 1$.

For D FFs, "Q follows D."

Hence, $Q_1^* = 1$ and $Q_0^* = 1$, which is state "3".

So, we know that "2" will go to "3".

The complete state diagram is

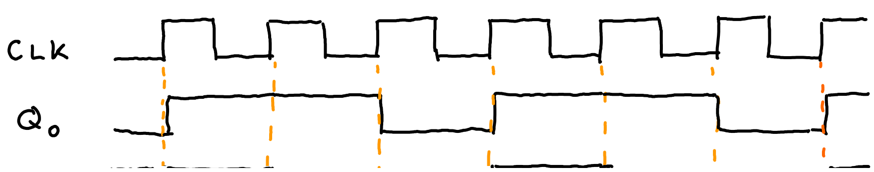


(4) If we assume that the counter start from state "2", then, from the state diagram that we derived in problem (3) we know that the counting sequence is

$$2 \to 3 \to 1 \to 0 \to 3 \to 1 \to 0 \to \cdots$$

This is the counting sequence; not the state diagram!

The waveform is drawn below:

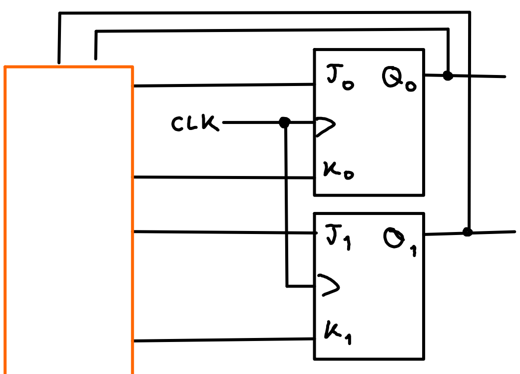


(5) The solution for this problem starts the same way as problem (2) upto the point where we have the next-state table:

$Q_1 Q_0$	$Q_1^* Q_0^*$
0 0	1 1
0 1	0 0
1 0	X X
1 1	0 1

The difference between this problem and problem (2) is that we are now required to use JK FFs instead of D FFs.

So, the circuit would be:



Our job is to determine the combinational circuit inside this box. Again, this box take the current $Q_1 Q_0$ value and then compute appropriate J_1, K_1, J_0, K_0 value so that the next Q's ($Q_1^* Q_0^*$) are correct.

We will use the excitation table to help us determine the input to the JK FFs.

$Q_1\ Q_0$	$Q_1^*\ Q_0^*$	$J_1 K_1$	$J_0 K_0$
0 0	1 1	1 X	1 X
0 1	0 0	0 X	X 1
1 0	X X	X X	X X
1 1	0 1	X 1	X 0

Excitation table for JK FFs

Q	Q^*	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

These are all X because we don't care about where state "2"

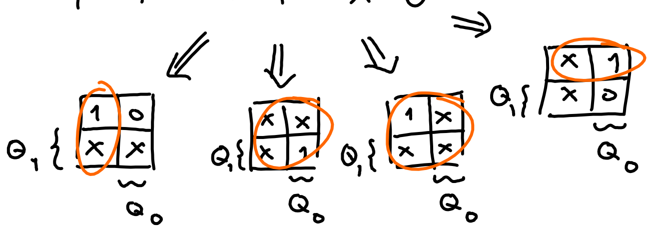
To get this, we first look at Q_1 and Q_1^* for this row.
We notice that $Q_1 = 0$ and $Q_1^* = 1$.
From the excitation table we must have $J_1 = 1$, $K_1 = X$.

will go next.

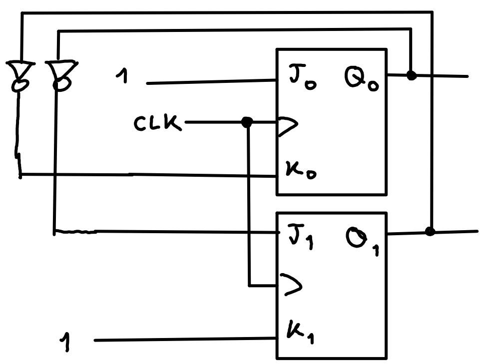
Note that all index are the same. That is, we are working with the FF labeled "1".

We can then copy down the truth table for the orange box above:

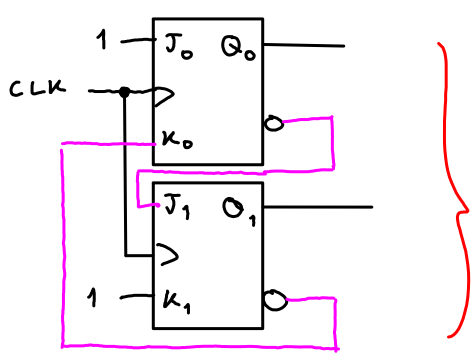
Q_1	Q_0	J_1	K_1	J_0	K_0
0	0	1	x	1	x
0	1	0	x	x	1
1	0	x	x	x	x
1	1	x	1	x	0



K-maps give $J_1 = \overline{Q_0}$, $K_1 = 1$, $J_0 = 1$, $K_0 = \overline{Q_1}$



If your JK FFs has the $\bar{Q}$ output, then we can eliminate the two NOT gates as followed:



Ans

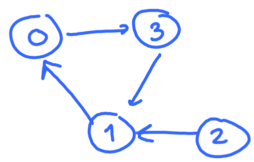
Note that when $Q_1 = 1$ and $Q_0 = 0$ (we are at state "2")

$$\underbrace{J_1 = \overline{Q_0} = 1,\ K_1 = 1}_{\text{toggle mode}},\ \underbrace{J_0 = 1,\ K_0 = \overline{Q_1} = 0}_{\text{SET mode}}$$

Hence $Q_1^* = 0$ and $Q_0^* = 1$

So, state "2" will go to "1" on the next clock pulse.

The "complete" state diagram is shown below:



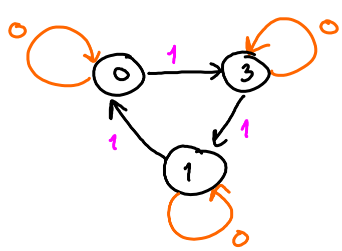
(6) The purpose of the count enable (CTEN) is to allow us to stop (hold) the counting.

For every clock pulse, we check the value of CTEN.

When CTEN = 1, the counting goes according to what we had in problem (2).

When CTEN = 0, the counting STOP and we sit at the same state.

The new state diagram become



In this case we want to modify circuit in problem (2) so that it take into accont the CTEN signal.

Back in problem (2) we have

$$D_1 = \overline{Q_0} \quad \text{and} \quad D_0 = \overline{Q_0} + Q_1 .$$

Because in problem (2), the counting always continue, the above equations should hold for us in the case that CTEN = 1.

(In other words, if CTEN is always "1", then we would observe exactly the same output as in problem 2.)

When CTEN = 0, we want to hold the value. So,

$$Q_1^* = Q_1 \quad \text{and} \quad Q_0^* = Q_0 .$$

To do this, because $Q^* = D$ for D FF, we connect

$$D_1 = Q_1 \quad \text{and} \quad D_0 = Q_0 .$$

Hence, we have two cases:

when CTEN = 1, $D_1 = \overline{Q_0}$ and $D_0 = \overline{Q_0} + Q_1$

when CTEN = 0, $D_1 = Q_1$ and $D_0 = Q_0$

These can be combined into

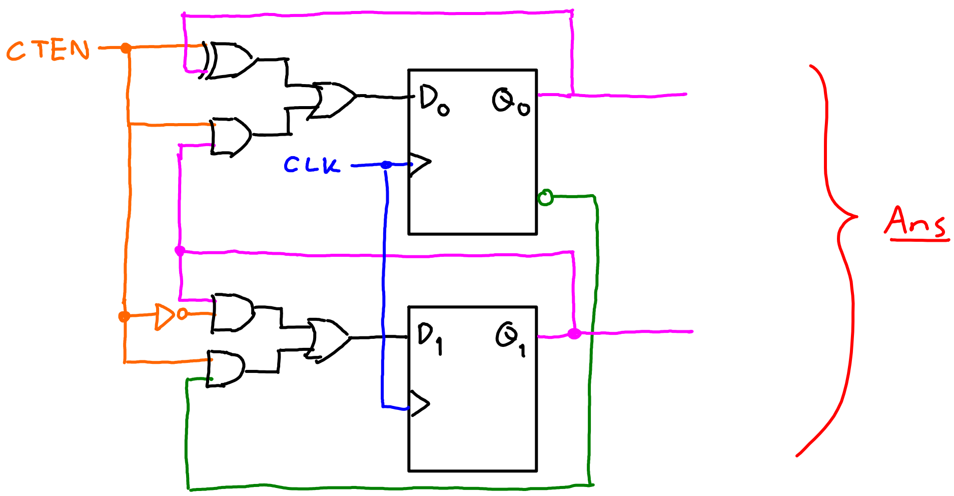
$$D_1 = CTEN \cdot \overline{Q_0} + \overline{CTEN} \cdot Q_1$$

$$D_0 = CTEN \cdot (\overline{Q_0} + Q_1) + \overline{CTEN} \cdot Q_0 = CTEN \oplus Q_0 + CTEN \cdot Q_1$$

I simplify it one more step.

(You can check them by letting CTEN = 0 or by letting CTEN = 1)

The modified circuit become



7 This is the same as problem 6 except that we now have to deal with JK FF.

It turns out that this case is even easier.

When CTEN = 1, we keep the same connection. (eg. for J_1, it is $\overline{Q_0}$)

When CTEN = 0, we want to hold and therefore all J, K values must be 0.

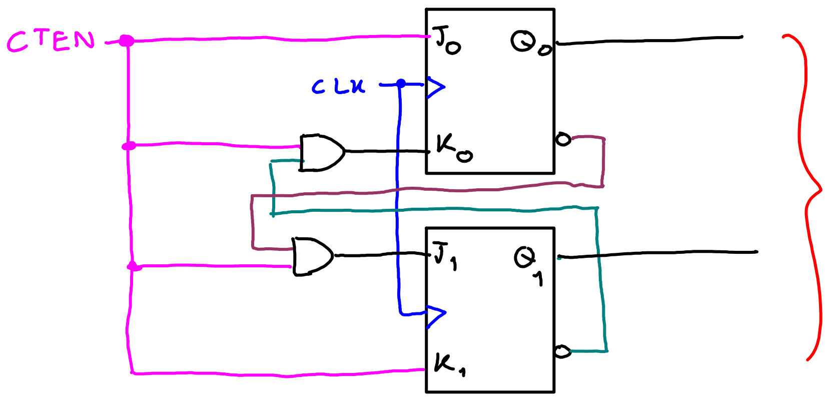
Hence, the combined expression is

$$J_0 = CTEN \cdot 1 + \cancel{\overline{CTEN} \cdot 0} = CTEN$$

$$K_0 = CTEN \cdot \overline{Q_1} + \cancel{\overline{CTEN} \cdot 0} = CTEN \cdot \overline{Q_1}$$

$$J_1 = CTEN \cdot \overline{Q_0} + \cancel{\overline{CTEN} \cdot 0} = CTEN \cdot \overline{Q_0}$$

$$K_1 = CTEN \cdot 1 + \cancel{\overline{CTEN} \cdot 0} = CTEN$$



Ans

Part B

18 I will only show the necessary steps in this problem.

First, we construct the next-state table:

Q_1	Q_0	Q_1^*	Q_0^*	J_1	K_1	J_0	K_0
0	0	1	0	1	X	0	X
0	1	1	1	1	X	X	0
1	0	0	1	X	1	1	X
1	1	0	0	X	1	X	1

Then, we use excitation table to find the appropriate excitation inputs J_1, K_1, J_0, K_0

This becomes the truth table for the circuit that produces J_1, K_1, J_0, K_0.

The corresponding K-maps are

	1	1
Q_1	x	x
		Q_0

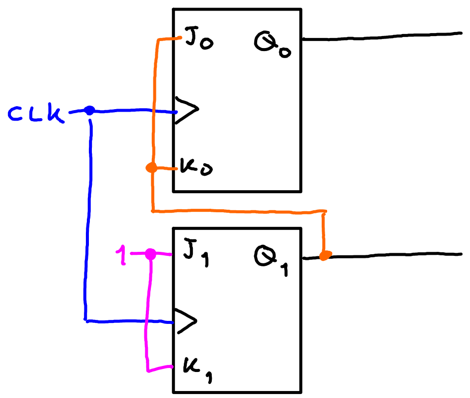
	x	x
Q_1	1	1
		Q_0

	0	x
Q_1	1	x
		Q_0

	x	0
Q_1	x	1
		Q_0

$J_1 = 1$ $\qquad K_1 = 1$ $\qquad J_0 = Q_1$ $\qquad K_0 = Q_1$

Hence, the circuit for the counter is



Ans